Your new problems on coding

Question 18. Is it possible to achieve in practice those actual MTD advantages with respect to other methods on efficiency and throughput at some decimal powers (100 - 1000 times!), which ones formally follow from estimations for a hardware decoder project?

Yes, it is. The unconditional regularity of our approach to estimations of hardware decoding efficiency is doubtless. It consists simply that as contrasted to all other methods our MTD contains as though only of shift registers, which ones are the most fast elements of any LSI circuit. Besides it is a lot of such registers working in parallel mode in MTD: from 4 up to 20 and more. And since customary speeds of shift registers of PLIS are tens Mbit/s, MTD decoders really are devices, which ones easily process flows at speeds in many hundreds Mbit/s.

Certainly, the problem is what do other devises of the MTD decoder do? You see it is necessary to make the solutions on which symbols should be changed. Process of decoding - is always a very difficult computing problem. Why then: "MTD is the only shift registers!"? Yes, because really active schemes of MTD are only threshold switches (TS). They are - extremely simple devices for integers addition and comparison with threshold values. Their quantity is very small as contrasted to tens and hundreds kbits of register memory. And it means, that in MTD ideal full multisequencing of operations is probable: creation of large number separately working TS. And the last major moment: all this set of TSs can easily be made by the schemes, which one will be looked outwardly as processors with the instantaneous answer: have shifted the data in the register - and here have received reacting of TSs, answer, whether it is necessary to change a controlled symbol. It is possible and even it is simple enough, as all TSs simply summarize some small integers. And for other algorithms of any such capabilities for superfast decoders organization in general are absent. That's all about throughput.

And if to return to a problem of efficiency, it is possible simply to remind, that MTD - iterative algorithm, which one at all changes of controlled

symbol strictly comes closer to the solution of the optimum decoder (OD). And this process can be realized at very low signal-to-noise ratios.

This two factors also determine MTD success: extremely fast decoding of lengthy codes with results, in many cases corresponding to optimum decoding by yardstick of a signal-to-noise ratio in a channel.

In particular, when simplest PLIS is taken even without usage of code concatenation MTD is created with speed more than 150 Mbit/s and with a code gain (CG) about 7,5 dB.

Moreover, the very precise technological simulation of MTD work in concrete PLIS has shown, that at small increase of chip capacity it provides even more high processing rate of and CG more than 8 dB, being non-concatenated circuit. Let's remark, that such a CG level corresponds to efficiency of a standard concatenated circuit with Viterbi algorithm (VA) and a code Read - Solomon.

So everything that was written earlier about MTD capabilities started with the most actual estimations and circumstances of a coding equipment design.

And about concatenated circuits with MTD usage it is possible to talk separately.

Question 19. Is it possible to use MTD in high velocity transmission systems at 60 Mbit/s? And at speed 400 Mbit/s? Well, and if it is else higher? And in general, what are maximum speeds of its work?

We should note, that problems of this type in such or in the similar forms about MTD we hear during many years. We supposed, that the similar problems of transmitting rates growth in general are not connected in any way with multithreshold algorithm. However just these problems arise often very much. Therefore we have decided they merit our attention.

We shall remind at first, that MTD is, as other methods of decoding, processing technique of digital streams, it is an algorithm. It can be characterized for software implementation by a main specification - number of operations per bit, and for hardware - directly by processing speed in Mbit/s.

As we have already told, the software MTD is customary at 2 decimal powers (~100 times!) more simple, than for close to it on efficiency methods of other type at enough large channel noise level. It means, that the usually microprocessor MTD implementation will be approximately in 100 times more fast. It very seldom happens in a modern history of development of data processing. In the field of decoding it was never occurred at all and, probably, it will never happen hereafter. We have already placed on educational pages of our site such a superfast MTD demoprogram. You can copy it into your

computer and try to play with it at miscellaneous tuned up parameters of a code, decoder and channel with Gaussian and packet components of a noise.

We have already created software MTD for a special digital TV system, in which one it has demonstrated in the next time its absolute advantage with respect to other coding systems.

At last, we have publications on throughput comparison of software versions of   different algorithms, which ones have allowed us to make introduced here conclusions. These articles and reports are indicated in lists of our papers on MTD subject. The full texts of some of them are placed on our site www.mtdbest.iki.rssi.ru .

From here it directly follows, that software MTD is always much more fast than other methods.

Now we approach to digits, which ones were indicated in a question. Their concrete values will depend on the microprocessor throughput. It is possible to proceed from costs about 60-300 operations per bit in MTD. Besides it is possible to admit, that "overhead expense", i. e. additional operations of the processor (calculus of indexes of arrays and so on) increase costs of the calculator approximately in m=3 of time. But, on the other hand, some processors allow to execute up to 8 commands simultaneously. And it picks up MTD throughput approximately in the same times. Certainly, they suppose, that the algorithm MTD easily enables good multisequencing of calculus. In the answers to earlier questions on codes we have shown that it is true indeed.

Now we can result an example of MTD throughput estimation. Let there is a processor with clock rate F=200 MHz. If we shall select algorithm MTD with complexity about n=100 of operations per bit, and an overhead expense we shall estimate on the average as triple (m=3), the throughput N for such MTD will be peer N=F/n/m=2*E8/100/3 ~670 Kbps. If they admit a capability of commands multisequencing of   such a processor in 8 times, then N~5 Mbit/s. And for microprocessor with clock rate ~1 GHz and without multisequencing they get N > 3 Mbit/s.

The experience has shown also, that for many personal IBM-compatible computers   the overhead expense can correspond   on the miscellaneous causes to parameter   m~6.

We think, that the proposed estimations and placed on our web-site superfast demoprogram MTD are sufficient for you to accept the exact solutions about using of microprocessor versions of a multithreshold decoder type.

The discussion of hardware versions MTD always is much more composite problem. But the detail analysis their throughput was already held as the answers on the previous questions. Therefore we shall remind only that it is completely correct to consider, that the MTD throughput in a hardware kind is determined by speed of shift registers data movement, which ones

usually are   the most fast schemes of microelectronics. Usually shift rates 30 - 100 Mbit/s in such registers are easily accessible. And since in MTD there can be even more than 20 such registers, working in parallel form, throughput which   one is   essentially more large, than 500 Mbit/s in hardware MTD appears quite accessible purpose. Thus, answer to a problem on speed of hardware MTD   is also quite positive for   all really asked coding system parameters.

<div align="center">* * *</div>

<u>The total of our discussion actually is   very simple.</u> Let there is hardware, which one is created to form the initial data flows for transmission and for the subsequent reception and processing, which one is characterized by certain throughput and definite level of development of element base. Then it is quite logical to use for the decoder components of the same level of throughput. It also allows to remove all doubts about a capability of MTD implementation with demanded throughput.

And, certainly, with growth of speeds of microelectronics MTD throughput will also quickly increase.

<div align="center" style="color:blue;">We invite you to send new questions on codes</div>